[METHOD AND SYSTEM FOR PERFORM-ING STATIC TIMING ANALYSIS ON DIGI-TAL ELECTRONIC CIRCUITS]

Abstract

A method for performing static timing analysis on digital electronic circuits is disclosed. A snip (or DC adjust) file is initially generated. Static timing analysis is then performed on the final circuit netlist using the snip file. If the final circuit netlist meets all the timing constraints, the snip file is converted to a group of cutpoints, and formal verification is performed on the cutpoints. A determination is made as to whether or not the cutpoints pass formal verification. If the cutpoints pass formal verification, the user analysis on the final circuit netlist is completed, and the final circuit netlist can proceed to manufacturing. Otherwise, if the cutpoints do not pass formal verification, a flag is issued to alert a user. The user then has to either modify certain snip point(s) within the snip file or modify the circuit netlist, and perform the user analysis again.